FPGA implementation of Real Time Switch for High precision based PROFINET-RT protocols.

Abstract— Industrial automation demands high precise synchronization between PLCs and Slave devices. PROFINET-RT specification demands cycle time of 31.25us. We at ATOP Technologies, have used high speed XILINX ZYNQ FPGA to achieve the required cycle time. The data received from PLC is first processed by Ethernet MAC IP, the redundant and netload frames are discarded at MAC layer. The received data are then processed on the Programmable logic side of FPGA. The processed data are then forwarded to next node which are connected in line topology. If the frame is intended to our node, the data is forwarded to Software stack or to the next node. The response frame received from stack is sent to PLC. Achieving the cycle time of 31.25us is practically possible using the Real time switch developed within FPGA.

ATOP Technologies, has developed the real time switch consisting of cut through. The local buffering of Ethernet frame is achieved using BRAM's for cut-through mode whereas, Ethernet frame can be forwarded to external DDR memory through DMA for Processor Subsystem (PS). The buffering technique helps the RT switch to meet the cycle time requirement of 1ms. Cut-through mechanism is used to send the frames to next nodes. Store-and-forward switching techniques are out of scope of this paper. With in-house developed FPGA logic, ATOP Technologies has been able to implement 2-port real time switch. PLC connectivity is transparent and agnostic to any of 2-Ports. Auto-negotiation is enabled in external PHY and provision is given to configure the PHY via management interface (MDIO/MDC). Frame received from PLC are expeditiously forwarded to the next downstream node. FPGA logic has helped to achieve required response time of PROFINET-RT protocol. The necessary software stack is ported on Processing Subsystem (PS) of FPGA. The Real time switch involves Frame filtering and identifying the Ethernet port details for each incoming frame. The complete logic is created as IP core, and can be easily ported on any of the XILINX SoC based devices. The protocol also adheres to IEC 61158-6-10. The RT switch is proven on ZYNQ 7020 evaluation boards and is also proven on ATOP's custom ZYNQ 7007 DI1000D board. The RT switch IP can be used on any of the processor-based XILINX FPGA device.

Keywords— PROFINET-RT, Real-time switch, FPGA, Cycle time, XILINX, PLC, Programmable logic, MAC, IEC, ZYNQ, Cut through switch, store and forward switch, PS, PL, MII, MDIO, MDC.

I. INTRODUCTION

Nowadays, Ethernet plays prominent role in industrial automation industry. Ethernet is not a real time communication protocol, but by making modification we can use Ethernet for real time communication. In Industrial automation, the requirement for field devices to support one of the field bus technologies have become priority and technological trend. Few of the field bus technologies include EtherCAT, Ethernet/IP, PROFINET-RT, PROFINET IRT, Modbus-TCP etc. Generally, there will be separate hardware and software chip. Communication between these chips is external. In this paper, protocol functionality has been implemented on Xilinx SoC based FPGA device and communication between hardware and software is internal to chip.

This paper focus on implementation of FPGA based Ethernet switch for PROFINET-RT protocol. PROFINET is Industrial Ethernet based communication, which adheres to IEC 61158 and IEC 61784 standards [1]. PROFINET supports high speed I/O process Real Time (RT) data. In automation industry, achieving cycle time of less than 1ms is top priority and equally highly challenging. Achieving this latency helps the industries to have more frequent access to motion control, critical IO devices etc. Hence, to configure or monitor the status of the devices on frequent basis may help in reducing the failure and recovery time to greater extent.

Traditionally, PLC encodes Ethernet packets to embed PROFINET-RT packets and sends to slaves as shown in "Fig.1". ATOP's IO slave devices in-turn are connected in network topology with monitoring and controller devices such as PLC. In order to achieve higher performance and required response time for PROFINET-RT protocol, time-critical functionality is to be implemented on programmable logic side of Xilinx Zynq SoC based FPGA devices.

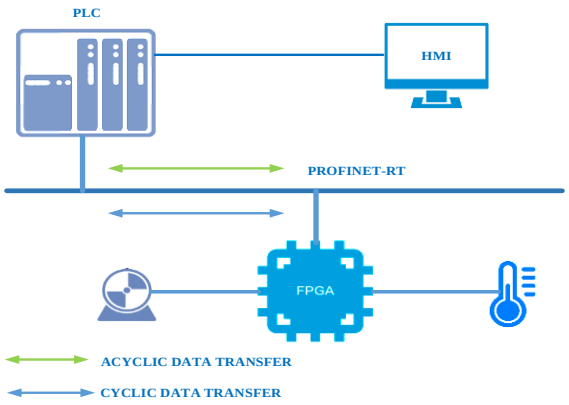

Fig. 1. Data Flow between PLC and PROFINET-RT devices.

Industrial applications mostly demand real time Ethernet device. PROFINET IO device uses Ethernet managed switch logic to route the packets between the ports. Currently PROFINET-RT uses managed switch characteristic. By implementing this switch logic on FPGA, it is possible to meet the tight timing constraint and high throughput [2]. This paper illustrates the PROFINET-RT switch, that gives real time communication services. The present switch module is based on cut-through switching mechanism which involves FIFO's logic. Compared to store and forward switching technique, implementation of cut-through switching logic provides high throughput, less latency and relatively less resource area on FPGA.

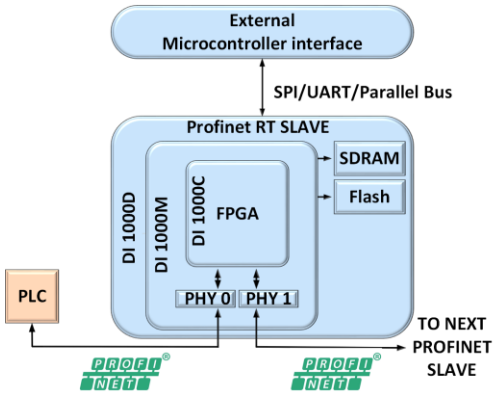

Fig. 2. ATOP PROFINET-RT Block Diagram.

"Fig. 2", depicts the high-level system block diagram of ATOP's FPGA based PROFINET-RT implementation on high end Zynq FPGA.

II. COMMUNICATION

PROFINET-RT PLC or IO-Controller is accompanied by general station description (GSDML) files so the IO-Devices can be configured for system engineering. The contents of the GSDML will be given with configuration information, parameters, modules, diagnostic, alarms, vendor and device identification information. With this information communication paths will be established between the IO-Controller and an IO-Device as shown in "Fig. 3", during system startup [3].

Communication between IO-Controller, and ATOP's IO slave Device is established, for cyclic and acyclic IO data exchange and for reading and writing record data explicitly using application relationship (AR) and Communication relations (CR).The send cycles are defined in GSDML file of the device and is configured by the engineering tool for each device.

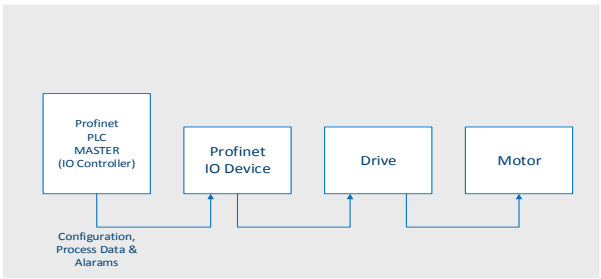

Fig. 3. Communication Path for PROFINET.

In this paper, PROFINET-RT switch logic on the PL side of FPGA has been implemented in such way that Ethernet packets from PLC are received through external Ethernet PHY and internal Xilinx soft EMAC IP core. Then, packets are decoded based on ether type of Ethernet frame and decision is taken to either forward to DMA or to the next downstream node. PROFINET-RT frames are buffered on external DDR-2 memory through Xilinx AXI-DMA controller IP which are then accessed by PROFINET-RT stack on the PS side. The PROFINET-RT Stack and drivers are used to drive the application device such as motor or sensors. "Fig. 4" shows the implemented view of PROFINET-RT and the communication mechanism between Programmable Logic and Processor System.

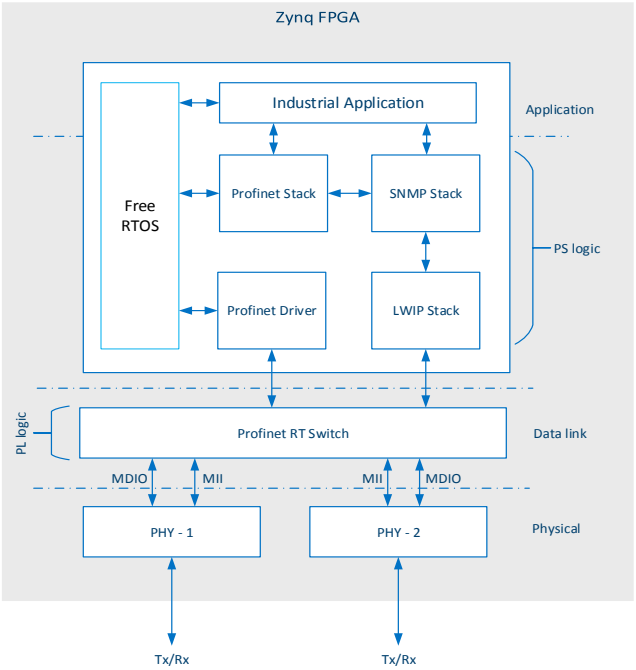

Fig. 4. Architecture PROFINET-RT Slave.

III. PROFINET-RT SWITCH MODULE IMPLEMENTATION

Verilog RTL code is used for design and implementation of FPGA logic and functional verification. The physical layer PHY receives the Ethernet frames and extracts the relevant information and forwards it to data link layer (where our PROFINET-RT switch module is implemented) and switch module sends that information to upper layer i.e. stack. ATOP's 2-PORT switch is implemented in such a way that either of the ports can act as master or slave with respect to PLC. PROFINET-RT protocol implementation uses a specialized Ethernet Media Access Control (Ethernet MAC) IP provided by XILINX and it is compatible to Media Independent Interface (MII) Standard. Interface of MII is running at 25Mhz.

Our switch module is implemented in such a way that the packets should reach the next node, depending on destination address and ether type in Ethernet packets. The generic Priority multiplexer and packet processing logic block as shown in "Fig 5", will make sure the switching activity to be traversing in the right direction and to right port. The Condition is such that, If PORT2 as well as DMA wants to send the data to PORT1, then Priority multiplexer chooses the data based on priority and data availability.

Finite state machine details of PROFINET-RT real time switch for cut-through mode is Shown in "Fig.6". State description and logic conditions of FSM logic are shown in Table1 and Table2.

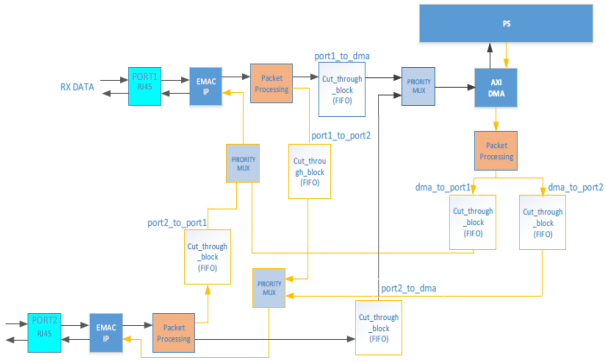

Fig. 5. Switch Block Diagram.

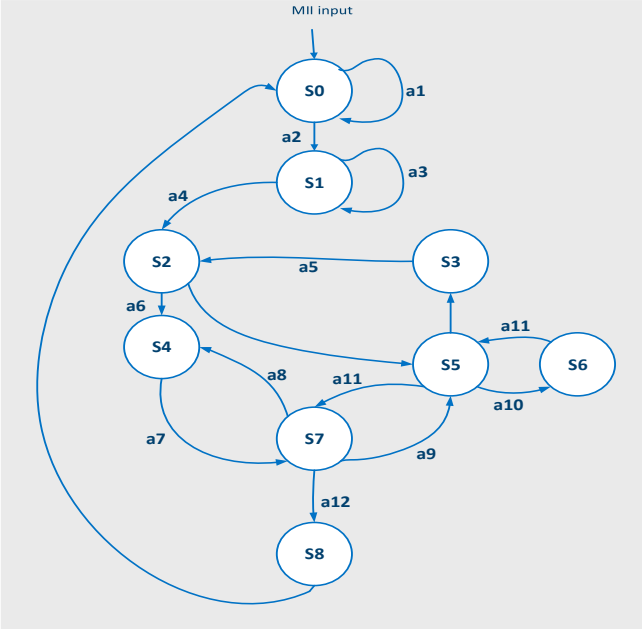

Fig. 6. Finite State machine of Switch Logic.

Table 1. Finite State Machine State description.

States	Description
S0	Idle
S1	EMAC IP Core
S2	Comparison logic
S3	PS reset register
S4	Store in cut through FIFO's
S5	Processor Subsystem
S6	Software stack and drivers
S7	Decision and Priority logic
S8	Port 2

Table 2. Condition of FSM Transition.

Logic Condition	Description
a1	MII signals valid check, if error discard.
a2	If valid then given to EMAC subsystem for CRC check.
a3	If invalid discard those packets.
a4	Compare source and destination address, Ether Type and reset by PS.
a5	Check reset will be given by PS.
a6	Store in Cut through FIFO's.
a7	Depending on comparison logic block decision taken to forward to DMA, Port2 or both ports.
a8	Data is read out only when tready signal from DMA/PORT2 is high.
a9	If intended to particular node Stack and drivers from PS side will process the request.
a10	Instructions to application device are extracted from frame and action will be taken by drivers.
a11	response from application device will be processed and action will be taken.
a12	If intended to port 2 then repeat the same process.

A. *Ethernet MAC IP*

EMAC IP core provides Ethernet functionality. EMAC supports MII interface to PHY chip [6]. The PHY is configured via management interface (MDIO/MDC) lines with auto negotiation enabled. The data transfer in this implementation occurs through MII interface at rate of 100Mbps. FPGA have two Ethernet port directly associated to the two Xilinx EMAC IP core fully adheres to IEEE 802.3 standard. In our switch module implementation, EMAC core is completely implemented on Programmable logic of FPGA, and gives us the following interfaces,

- Ethernet PHY MII (Media independent Interface) interface.
- Transmission control and data ports.

The TX and RX memory size of EMAC IP is selected for 4K. The Master PLC sends data in Ethernet frame format, EMAC IP receives the data through MII lines and process the data. EMAC IP functionality is to check whether the received frames are valid or invalid by using CRC mechanism. If the frame is valid it simply forwards to packet processing block, if it is not valid discards that frame.

B. *Packet Procssing*

The packet processing block receives the data from the EMAC and decodes the destination address and ether type and performs the below operation,

- If it's not Multicast/Broadcast frames and destination mac address is equal to read destination address register or LLDP - Sends the received data to stack side.
- If it's not Multicast/Broadcast frames and destination mac address is not equal to read destination address register or LLDP - Sends the received data to PORT2.
- If it's Multicast/Broadcast frames - Sends the received data to both PS side and PORT2.

C. *Cut-Through FIFO*

The processed data should not lose from the network, the received data is stored in FIFO, the data is read out only when tready signal from DMA/PORT2 is high. FIFO function is to store the packet and forward it to next node. Store and forward FIFO utilizes resource in FPGA because of its features. This FIFO stores complete packet and checks data integrity and forwards packet to next node. This FIFO is traditionally less latency. 32-bit wide and 2048-bit depth cut-through FIFO IP is instantiated. In Cut-through FIFO, forwarding packets to next node by just analyzing destination MAC. Cut-through FIFO offers best latency. Top level block diagram of cut-trough FIFO IP as shown in "Fig. 7".

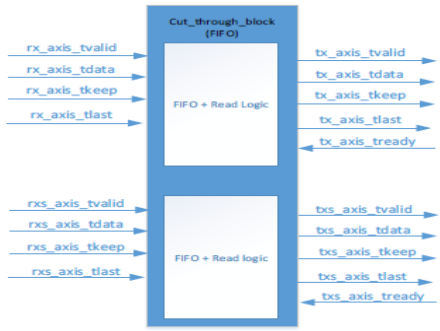

Fig. 7. Cut-Through FIFO.

IV. RESULT AND DISCUSSION

A. *DI1000D*

The Real time switch logic is ported on ATOP's development board, the board features are listed on "Fig. 8".

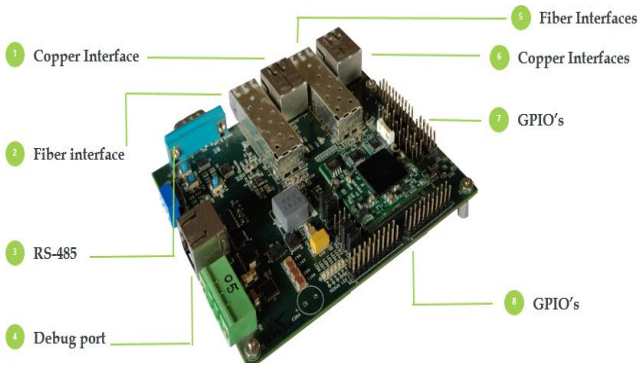

Fig. 8. ATOP's Development Board.

DI1000D is a custom-made development board by ATOP Technologies, which has two copper and fiber interface either of the 2-ports are compatible to be connected to the PLC. External GPIO ports are used for SPI, I2C, GPMC interface. There is a debug port for diagnosis. In this implementation DI1000M module is mounted on DI1000D board. The reset switches are present only on the based board.

B. *PROFINET-RT Switch Implementation*

Using the Xilinx vivado toolset, we have implemented PROFINET_RT switch module in a ATOP`s DI1000D custom made FPGA Board, which offers high performance. Zynq FPGA is mounted on DI1000D module. The Synthesis and route utilization shown in Table 3.

Table 3. Synthesis Resource Utilization Report.

Resource Type	**Utilization Amount**
Gate Count	13857
Memory Usage	1360K
Number of IO's	77
Number of registers	19319

C. *Simulation Waveform*

The "Fig. 9", simulation result is taken for PROFINET-RT switch module implementation. The packets are given through test bench. The packet switching between the ports depend on the transmission streams. Depending on the destination address of the IP packets, data will route to the destination port. Here in simulation waveform, where the signal tvalid of 1st EMAC IP, is transition from logic 0 to 1 indicates that the data transmission is happening. The signal m_axis_rxd_tdata contains the IP Packets which are received on PORT 1. After processing the IP Packet in our switch mechanism, the data are sent out from PORT 2 i.e. s_axis_txd_1_tdata. The Processing delay between the received and transmit of packets between the EMAC IP's is 140 ns, which is observed on functional simulation.

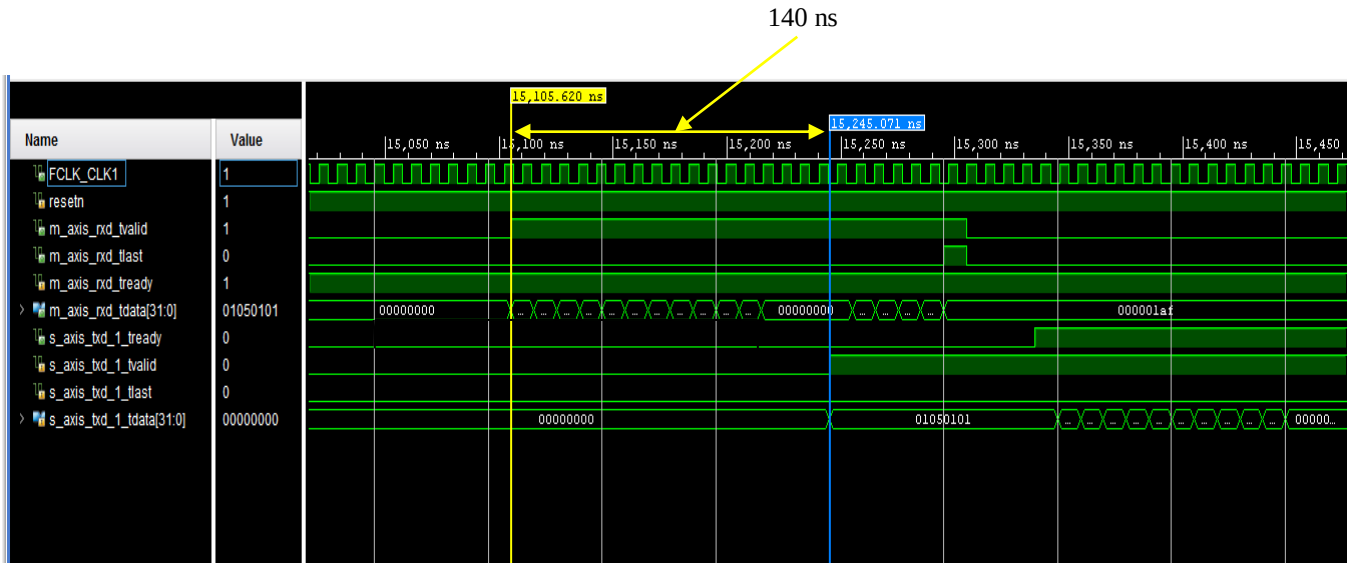

Fig. 9. Simulation Result for PROFINET Switch Logic on Xilinx Vivado Tool.

D. System level Test Setup and Validation

The PROFINET-RT test Setup and Configuration is shown in "Fig. 10". PC acts as Master, which sends Ethernet packets from Automated PNIO RT Tester toolset to the PROFINET-RT IO slave device. Scalance Switch is meant to connect multiple PROFINET-RT IO devices and enable to forward the received frame to next slave device. Different types of test cases are performed to validate the PROFINET-RT device. These test cases are explained below. Manual test is part of automated test suit released in September 2018 test IO-bundle for PNIO tester.

- Automated RT Tester.
- Security Level Test.
- TED Test Cases.

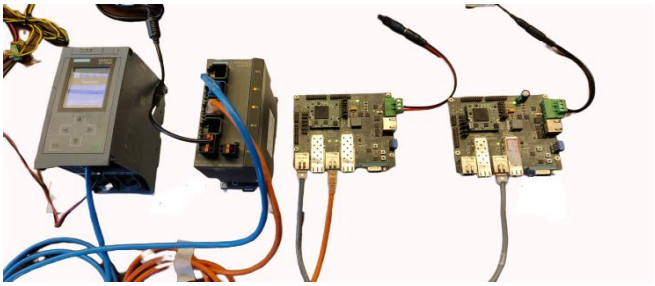
Fig. 10. PLC and Slave PROFINET-RT Setup.

The goal of the Automated RT Tester is to provide a test environment to validate the functionality of PROFINET-RT devices. Automated Test cases can be executed without any user interaction. Manual Test cases require user interaction to execute the test case completely. In order to achieve reproducible behaviours of PROFINET IO devices, the network load values supported by PROFINET IO devices must be considered in the certification process. To pass certification and as a precondition on issuing the certificate the device must at least pass the tests for "net load class I."

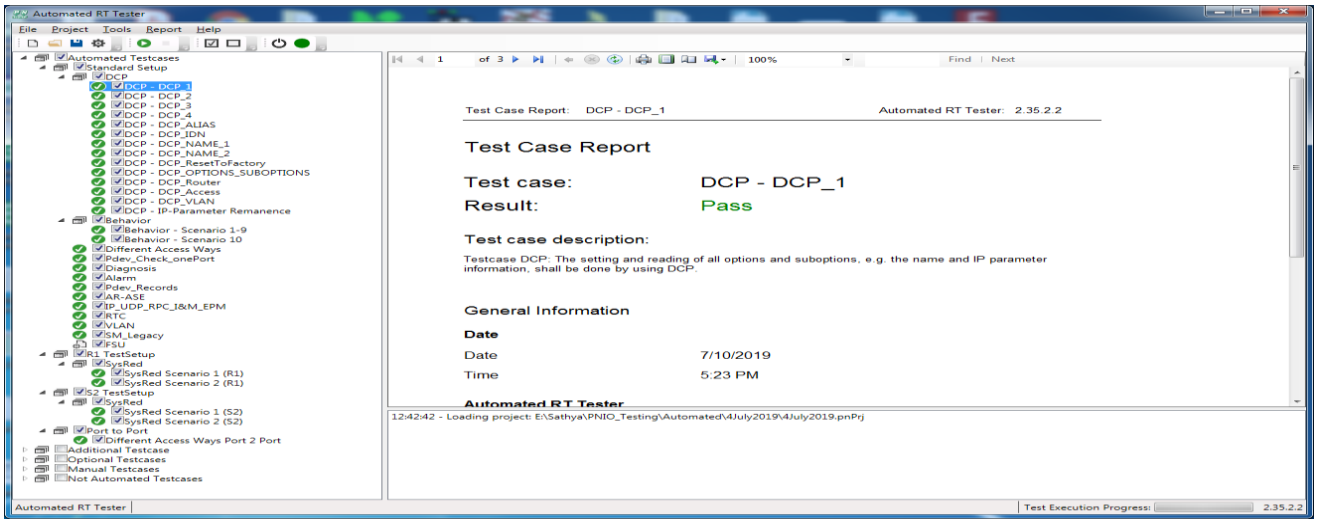

Fig. 11. Automated RT Tester Test Case Report.

E. FPGA hardware desin validation results

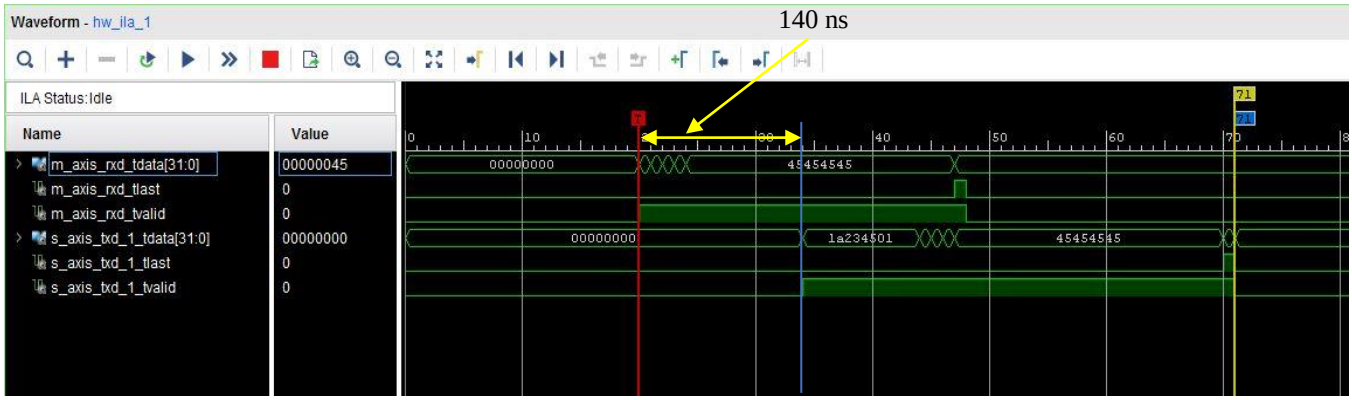

Fig. 12. FPGA Hardware Validation Chipscope Waveform.

No.	Time	Source	Destination	Protocol	Length	Info
10	10.197574	Siemens_4a:26:a8	LLDP_Multicast	PN-PTCP	80	DelayReq , Seq=1118, Delay= 0ns, PortMAC=20:87:56:4a:26:a8
11	11.397606	Siemens_4a:26:a8	LLDP_Multicast	PN-PTCP	80	DelayReq , Seq=1119, Delay= 0ns, PortMAC=20:87:56:4a:26:a8
12	11.671672	192.168.0.100	192.168.0.50	PNIO-CM	695	Connect request, ARBlockReq, IOCRBlockReq, IOCRBlockReq, ExpectedSubmoduleBlockReq, ExpectedSubmod…
13	11.675095	192.168.0.50	192.168.0.100	PNIO-CM	244	Connect response, OK, ARBlockRes, IOCRBlockRes, IOCRBlockRes, AlarmCRBlockRes, ARServerBlock
14	11.675790	AtopTech_00:02:04	Siemens_13:86:12	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
15	11.675801	192.168.0.100	192.168.0.50	PNIO-CM	437	Write request, IODWriteReqHeader, Api:0xffffffff, Slot:0xffff/0xffff, Index:MultipleWrite, 211 byt…
16	11.676993	Siemens_13:86:12	AtopTech_00:02:04	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
17	11.677873	AtopTech_00:02:04	Siemens_13:86:12	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
18	11.679118	Siemens_13:86:12	AtopTech_00:02:04	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
19	11.679150	192.168.0.50	192.168.0.100	PNIO-CM	418	Write response, OK, IODWriteResHeader, Api:0xffffffff, Slot:0xffff/0xffff, Index:MultipleWrite, OK…
20	11.679151	192.168.0.100	192.168.0.50	PNIO-CM	194	Control request, IODControlReq Prm End.req, Command: ParameterEnd
21	11.679773	AtopTech_00:02:04	Siemens_13:86:12	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
22	11.681200	Siemens_13:86:12	AtopTech_00:02:04	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
23	11.681872	AtopTech_00:02:04	Siemens_13:86:12	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
24	11.683194	Siemens_13:86:12	AtopTech_00:02:04	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
25	11.683783	AtopTech_00:02:04	Siemens_13:86:12	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)
26	11.685198	Siemens_13:86:12	AtopTech_00:02:04	PNIO_PS	80	RTC1, ID:0x8000, Len: 60, Cycle:47617 (Invalid,Backup,Problem,Stop)

Fig. 13. Wireshark Capture

F. PROFINET Packet analysis for FPGA logic

Wireshark, an open source windows software, is used for packet analyzing and capturing of live network traffic. In our implementation, we used this software to check the packet loss. After slave receives the packet from master PC, slave acknowledges with response frame back to the PC. “Fig. 13”, shows the screenshot capture of PROFINET-RT packet analysis.

V. CONCLUSION

With the help of FPGA reprograming capability and Programmable logic and Processing system compatibility, implementing switch logic in FPGA helps the automation industry for future renovations. The Real-time PROFINET-RT Switch module presented in this paper is a complete set of hardware and software unit. All the real-time requirements i.e. frame decode, packet processing logic and Priority multiplexer logic is implemented by using Verilog RTL. By implementing PROFINET-RT switch on FPGA, we have achieved total processing delay for forwarding the frame to the next downstream node in 140 ns. This paper describes the development and validation techniques of cut-through functionality between the nodes connected in line topology. The implemented Protocol is tested on Automated RT tester toolset, which adheres to IEC 61158 and IEC 61784 standards. The PROFINET-RT protocol has been and tested in provision with cycle time and accuracy.

ACKNOWLEDGMENT

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